19-2887; Rev. 3; 11/92

MAXIM

High-Speed, Low-Power Voltage Comparators

General Description

The MAX900-903 high-speed, low-power, single/dual/quad voltage comparators feature differential analog inputs and TTL logic outputs with active internal pull-ups. Fast propagation delay (8ns typ at 5mV overdrive) makes the MAX900-903 ideal for fast A/D converters and sampling circuits, line receivers, V/F converters, and many other data-discrimination applications.

All comparators can be powered from separate analog and digital power supplies or from a single combined supply voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. The MAX900-903 consume 18mW per comparator when powered from +5V.

The MAX900-903 are equipped with independent TTL compatible latch inputs. The comparator output states are held when the latch inputs are driven low. The MAX901 provides the same performance as the MAX900, MAX902, and MAX903 with the exception of the latches.

Applications

High-Speed A/D Converters
High-Speed V/F Converters
Line Receivers
Threshold Detectors
Input Trigger Circuitry
High-Speed Data Sampling
PWM Circuits

Features

- ♦ 8ns Typ Propagation Delay
- ♦ 18mW/Comparator Power Consumption (Typ at +5V)
- ♦ Separate Analog and Digital Supplies
- ♦ Flexible Analog Supply: +5V to +10V or ±5V
- ♦ Input Range Includes Negative Supply Rail
- ♦ TTL Compatible Outputs
- ♦ TTL Compatible Latch Inputs (Except MAX901)

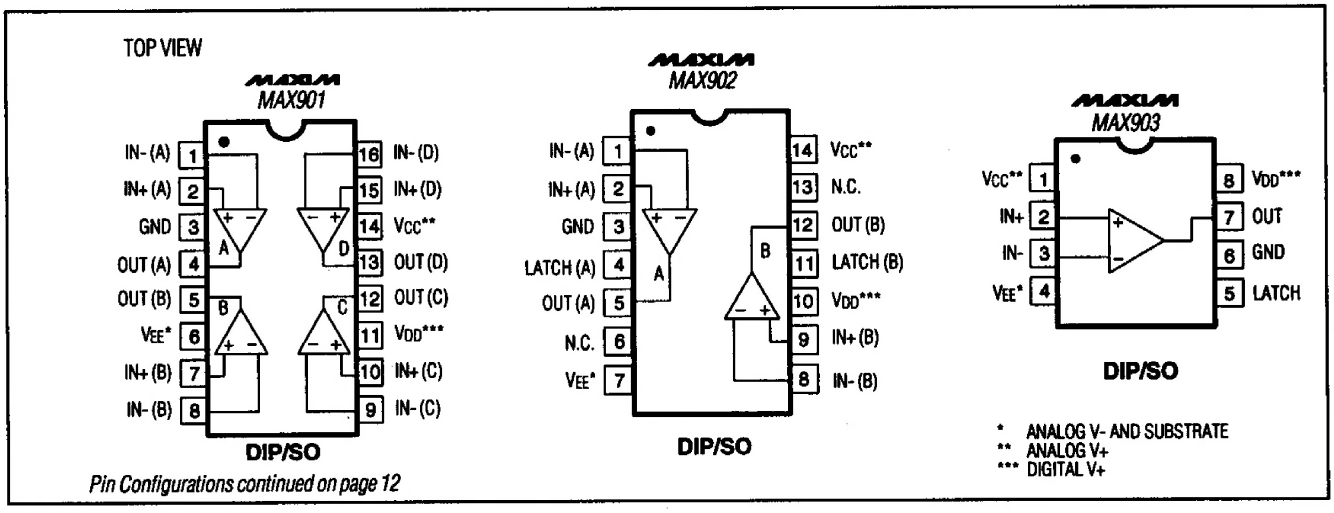
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX900ACPP	0°C to +70°C	20 Plastic DIP
MAX900BCPP	0°C to +70°C	20 Plastic DIP
MAX900ACWP	0°C to +70°C	20 Wide SO
MAX900BCWP	0°C to +70°C	20 Wide SO
MAX900BC/D	0°C to +70°C	Dice*
MAX900AEPP	-40°C to +85°C	20 Plastic DIP
MAX900BEPP	-40°C to +85°C	20 Plastic DIP
MAX900AEWP	-40°C to +85°C	20 Wide SO
MAX900BEWP	-40°C to +85°C	20 Wide SO
MAX900AMJP	-55°C to +125°C	20 CERDIP
MAX900BMJP	-55°C to +125°C	20 CERDIP

Ordering Information continued at end of data sheet.

*Contact factory for dice specifications.

Pin Configurations



Pin Configurations continued on page 12

High-Speed, Low-Power Voltage Comparators

ABSOLUTE MAXIMUM RATINGS (Note 1)

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{DD} to GND) ..... +7V
Differential Input Voltage ..... [V_{EE}-0.2V] to [V_{CC}+0.2V]
Common-Mode Input Voltage ..... [V_{EE}-0.2V] to [V_{CC}+0.2V]
Latch Input Voltage (MAX900/902/903 only) -0.2V to [V_{DD}+0.2V]
Output Short-Circuit Duration
to GND ..... Indefinite
to V_{DD} ..... 1 min
Internal Power Dissipation 500mW
Derate above +100°C ..... 10mW/°C

Operating Temperature Ranges:
MAX900-903_C_ _ .....0°C to +70°C
MAX900-903_E_ _ ..... -40°C to +85°C
MAX900-903_M_ _ ..... -55°C to +125°C
Junction Temperature (Tj) ..... -65°C to +160°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	V_{CM} = 0V, V_O = 1.4V		0.5	2.0		1.0	4.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}		3	6		4	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V		50	250		100	500	nA
Input Voltage Range	V_{CM}	(Note 2)	V_{EE}-0.1		V_{CC}-2.25	V_{EE}-0.1		V_{CC}-2.25	V
Common-Mode Rejection Ratio	CMRR	-5V<V_{CM}<+2.75, V_O = 1.4V (Note 3)		50	150		75	250	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)		50	150		100	250	µV/V
Output High Voltage	V_{OH}	V_{IN}>250mV, I_{SRC} = 1mA	2.4	3.5		2.4	3.5		V
Output Low Voltage	V_{OL}	V_{IN}>250mV, I_{SINK} = 8mA		0.3	0.4		0.3	0.4	V
Latch Input Voltage High	V_{LH}	(Note 4)		1.4	2.0		1.4	2.0	V
Latch Input Voltage Low	V_{LL}	(Note 4)	0.8	1.4		0.8	1.4		V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V (Note 4)		1	20		1	20	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V (Note 4)		1	20		1	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Analog Supply Current	I_{CC}	(Note 8)		10	15		5	8		2.5	4	mA
Negative Analog Supply Current	I_{EE}	(Note 8)		7	12		3.5	6		2	3	mA
Digital Supply Current	I_{DD}	(Note 8)		4	6		2	3		1	1.5	mA
Power Dissipation	P_D	V_{CC} = V_{DD} = +5V, V_{EE} = 0V		70	105		35	55		18	28	mW

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input-to-Output High Response Time	t_{pd+}	V_{OD} = 5mV, C_L = 15pF, I_O = 2mA (Note 5)		8	10		8	10		8	10	ns
Input-to-Output Low Response Time	t_{pd-}	V_{OD} = 5mV, C_L = 15pF, I_O = 2mA (Note 5)		8	10		8	10		8	10	ns
Difference in Response Time Between Outputs	Δt_{pd}	(Notes 5, 6)		0.5	2.0		0.5	2.0		0.5	2.0	ns
Latch Disable to Output High Delay	$t_{pd+}(D)$	(Notes 4, 7)		10			10			10		ns
Latch Disable to Output Low Delay	$t_{pd-}(D)$	(Notes 4, 7)		12			12			12		ns
Minimum Setup Time	t_s	(Notes 4, 7)		2			2			2		ns
Minimum Hold Time	t_h	(Notes 4, 7)		1			1			1		ns
Minimum Latch Disable Pulse Width	$t_{pw}(D)$	(Notes 4, 7)		10			10			10		ns

Note 2: The input common-mode voltage and input signal voltages should not be allowed to go negative by more than 0.2V below V_{EE}. The upper end of the common-mode voltage range is typically V_{CC}-2V, but either or both inputs can go to a maximum of V_{CC}+0.2V without damage.

Note 3: Tested for +4.75V<V_{CC}<+5.25V, and -5.25V<V_{EE}<-4.75V with V_{DD} = +5V, although permissible analog power-supply range is +4.75V<V_{CC}<+10.5V for single-supply operation with V_{EE} grounded.

Note 4: Specification does not apply to MAX901.

Note 5: Guaranteed by design. Times are for 100mV step inputs (see propagation delay characteristics in Figures 2 and 3).

Note 6: Maximum difference in propagation delay between any of the four comparators in the MAX900/901/902/903.

Note 7: See Timing Diagram (Figure 2). Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in a production environment. Typical specifications listed are taken from measurements using a high-speed test-jig.

Note 8: I_{CC} tested for +4.75V<V_{CC}<+10.5V with V_{EE} grounded. I_{EE} tested for -5.25V<V_{EE}<-4.75V with V_{CC} = +5V. I_{DD} tested for +4.75V<V_{DD}<+5.25V with the worst-case condition of all four comparator outputs at logic low.

High-Speed, Low-Power Voltage Comparators

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High; T_A = Full Operating Temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	V_{CM} = 0V, V_O = 1.4V		1	3		2	6	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}		4	10		6	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V		100	500		200	800	nA
Input Voltage Range	V_{CM}	(Note 2)	V_{EE}-0.1		V_{CC}-2.25	V_{EE}-0.1		V_{CC}-2.25	V
Common-Mode Rejection Ratio	CMRR	-5V<V_{CM}<+2.75V, V_O = 1.4V (Note 3)		80	250		120	500	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)		100	250		150	500	µV/V
Output High Voltage	V_{OH}	V_{IN}>250mV, I_{SRC} = 1mA	2.4	3.5		2.4	3.5		V
Output Low Voltage	V_{OL}	V_{IN}>250mV, I_{SINK} = 8mA		0.3	0.4		0.3	0.4	V
Latch Input Voltage High	V_{LH}	(Note 8)		1.4	2.0		1.4	2.0	V
Latch Input Voltage Low	V_{LL}	(Note 8)	0.8	1.4		0.8	1.4		V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V (Note 8)		2	20		1	20	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V (Note 8)		2	20		1	20	µA

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Analog Supply Current	I_{CC}	(Note 8)		10	25		5	12		2.5	6	mA
Negative Analog Supply Current	I_{EE}	(Note 8)		7	20		3.5	10		2	5	mA
Digital Supply Current	I_{DD}	(Note 8)		4	10		2	5		1	2.5	mA
Power Dissipation	P_D	V_{CC} = V_{DD} = +5V, V_{EE} = 0V		70	105		35	55		18	28	mW

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input-to-Output High Response Time	t_{pd+}	V_{OD} = 5mV C_L = 15pF I_O = 2mA (Note 5)		10	15		10	15	ns
Input-to-Output Low Response Time	t_{pd-}	V_{OD} = 5mV C_L = 15pF I_O = 2mA (Note 5)		10	15		10	15	ns
Difference in Response Time Between Outputs	Δt_{pd}	(Notes 5, 6)		1	3		1	3	ns

Note 2: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.2V below V_{EE}. The upper end of the common-mode voltage range is typically V_{CC}-2.0V, but either or both inputs can go to a maximum of V_{CC}+0.2V without damage.

Note 3: Tested for +4.75V<V_{CC}<+5.25V, and -5.25V<V_{EE}<-4.75V with V_{DD} = +5V, although permissible analog power-supply range is +4.75V<V_{CC}<+10.5V for single-supply operation with V_{EE} grounded.

Note 4: Specification does not apply to MAX901.

Note 5: Guaranteed by design. Times are for 100mV step inputs (see propagation delay characteristics in Figures 2 and 3).

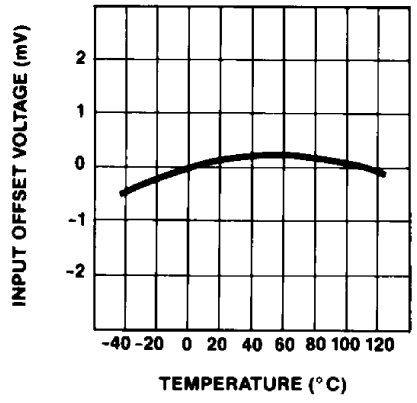
Note 6: Maximum difference in propagation delay between any of the four comparators in the MAX900/901/902/903.

Note 7: See Timing Diagram (Figure 2). Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in a production environment. Typical specifications listed are taken from measurements using a high-speed test-jig.

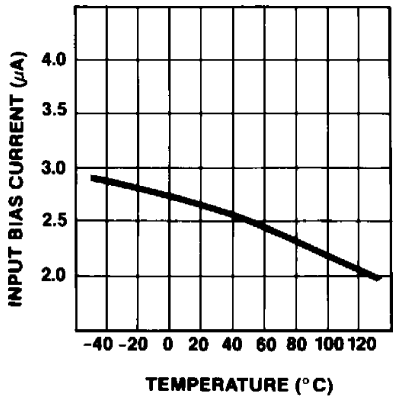
Note 8: I_{CC} tested for +4.75V<V_{CC}<+10.5V with V_{EE} grounded. I_{EE} tested for -5.25V<V_{EE}<-4.75V with V_{CC} = +5V. I_{DD} tested for +4.75V<V_{DD}<+5.25V with the worst-case condition of all four comparator outputs at logic low.

Typical Operating Characteristics

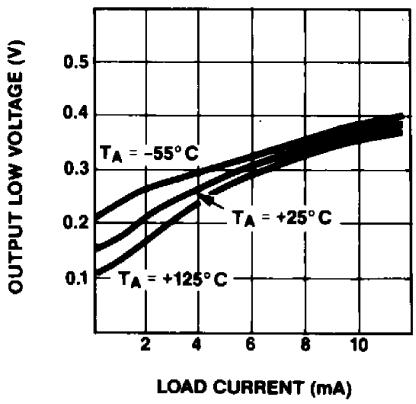
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



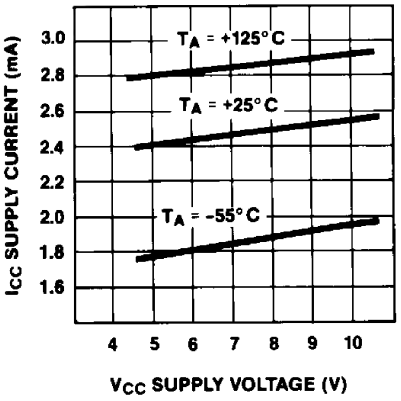
OUTPUT LOW VOLTAGE (V_{OL}) vs. LOAD CURRENT



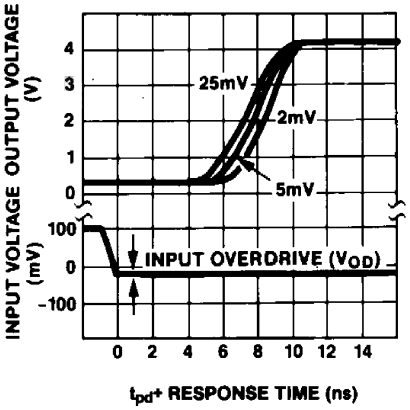
High-Speed, Low-Power Voltage Comparators

Typical Operating Characteristics (continued)

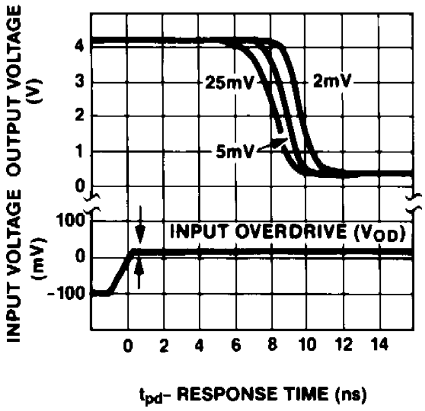
I_{CC} SUPPLY CURRENT (PER COMPARATOR) vs. V_{CC} SUPPLY VOLTAGE (V_{DD} = +5V)



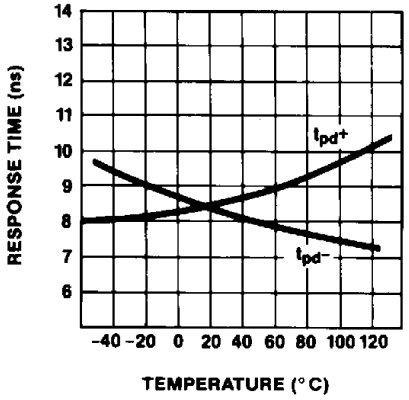
INPUT OVERDRIVE vs. t_{pd+} RESPONSE TIME



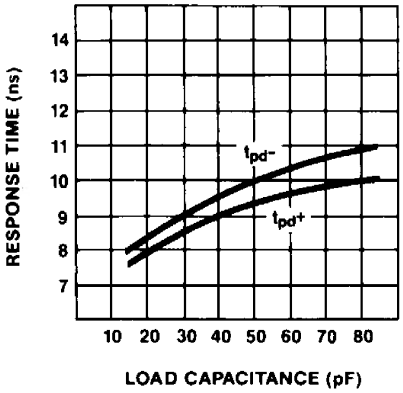
INPUT OVERDRIVE vs. t_{pd-} RESPONSE TIME



RESPONSE TIME vs. TEMPERATURE (5mV OVERDRIVE)



RESPONSE TIME vs. LOAD CAPACITANCE (5mV OVERDRIVE, R_{LOAD} = 2.4kΩ)



Pin Descriptions

MAX900

PIN	NAME	FUNCTION
1, 10, 11, 20	IN- (A, B, C, D)	Negative Input (Channels A, B, C, D)
2, 9, 12, 19	IN+ (A, B, C, D)	Positive Input (Channels A, B, C, D)
3	GND	Ground Terminal
4, 7, 14, 17	LATCH (A, B, C, D)	Latch Input (Channels A, B, C, D)
5, 6, 15, 16	OUT (A, B, C, D)	Output (Channels A, B, C, D)
8	V_{EE}	Negative Analog Supply and Substrate
13	V_{DD}	Positive Digital Supply
18	V_{CC}	Positive Analog Supply

MAX901

PIN	NAME	FUNCTION
1, 8, 9, 16	IN- (A, B, C, D)	Negative Input (Channels A, B, C, D)
2, 7, 10, 15	IN+ (A, B, C, D)	Positive Input (Channels A, B, C, D)
3	GND	Ground Terminal
4, 5, 12, 13	OUT (A, B, C, D)	Output (Channels A, B, C, D)
6	V_{EE}	Negative Analog Supply and Substrate
11	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

MAX902

PIN	NAME	FUNCTION
1, 8	IN- (A, B)	Negative Input (Channels A, B)
2, 9	IN+ (A, B)	Positive Input (Channels A, B)
3	GND	Ground Terminal
4, 11	LATCH (A, B)	Latch Input (Channels A, B)
5, 12	OUT (A, B)	Output (Channels A, B)
6, 13	N.C.	No Connect
7	V_{EE}	Negative Analog Supply and Substrate
10	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

MAX903

PIN	NAME	FUNCTION
1	V_{CC}	Positive Analog Supply
2	IN+	Positive Input
3	IN-	Negative Input
4	V_{EE}	Negative Analog Supply and Substrate
5	LATCH	Latch Input
6	GND	Ground Terminal
7	OUT	Output
8	V_{DD}	Positive Digital Supply

High-Speed, Low-Power Voltage Comparators

Applications Information

Circuit Layout

Because of the large gain-bandwidth transfer function of the MAX900-903, special precautions must be taken to realize their full high-speed capability. A printed circuit board with a good, low-inductance ground plane is mandatory. All decoupling capacitors (the small 100nF ceramic type is a good choice) should be mounted as close as possible to the power-supply pins. Separate decoupling capacitors for analog V_{CC} and for digital V_{DD} are also recommended. Close attention should be paid to the bandwidth of the decoupling and terminating components. Short lead lengths on the inputs and outputs are essential to avoid unwanted parasitic feedback around the comparators. Solder the device directly to the printed circuit board instead of using a socket.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of the MAX900-903 can create oscillation problems when the input traverses the linear region. For clean output switching without oscillation or steps in the output waveform, the input must meet minimum slew-rate requirements. Oscillation is largely a function of board layout and of coupled source impedance and stray input capacitance. Both poor layout and large source impedance will cause the part to oscillate and increase the minimum slew-rate requirement. In some applications, it may be helpful to apply some positive feedback between the output and + input. This pushes the output through the transition region cleanly, but applies a hysteresis in threshold seen at the input terminals.

TTL Output and Latch Inputs

The comparator TTL output stages are optimized for driving low-power Schottky TTL with a fan-out of four.

When the latch is connected to a logic high level or left floating, the comparator is transparent and immediately responds to changes at the input terminals. When the latch is connected to a TTL low level, the comparator output latches in the same state as at the instant that the latch command is applied, and will not respond to subsequent changes at the input. No latch is provided on the MAX901.

Power Supplies

The MAX900-903 can be powered from separate analog and digital supplies or from a single +5V supply. The analog supply can range from +5V to +10V with V_{EE} grounded for single-supply operation (Figures 1A and 1B) or from a split ±5V supply (Figure 1C). The V_{DD} digital supply always requires +5V.

In high-speed, mixed-signal applications where a common ground is shared, a noisy digital environment can adversely affect the analog input signal. When set up with separate supplies (Figure 1C), the MAX900-903 isolate analog and digital signals by providing a separate AGND(V_{EE}) and DGND.

Typical Power-Supply Alternatives

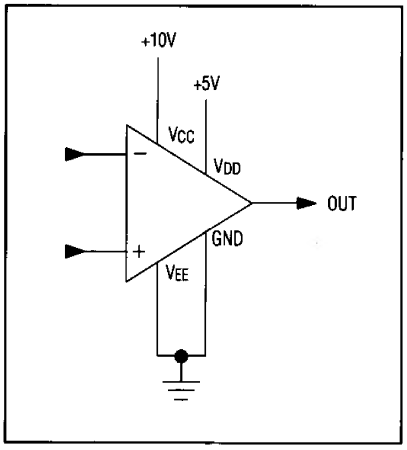


Figure 1A. Separate Analog Supply, Common Ground

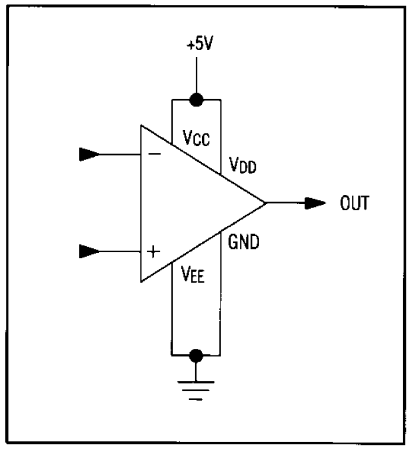


Figure 1B. Single +5V Supply, Common Ground

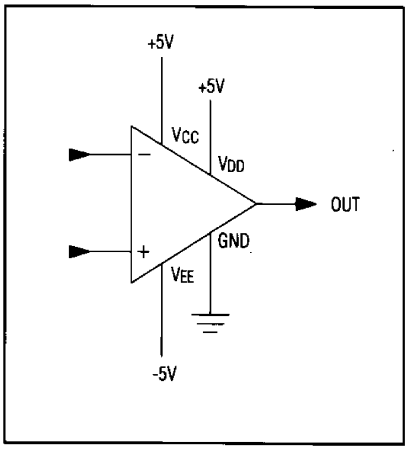


Figure 1C. Split ±5V Supply, Separate Ground

Definition of Terms

V_{OS} **Input Offset Voltage:** Voltage applied between the two input terminals to obtain TTL logic threshold (+1.4V) at the output.

V_{IN} Input Voltage Pulse Amplitude: Usually set to 100mV for comparator specifications.

V_{OD} **Input Voltage Overdrive:** Usually set to 5mV and in opposite polarity to V_{IN} for comparator specifications.

t_{pd+} Input to Output High Delay: The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold of an output low to high transistion.

t_{pd-} Input to Output Low Delay: The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold of an output high to low transition.

t_{pd+} (D) Latch Disable to Output High Delay: The propagation delay measured from the latch signal crossing the TTL threshold in a low to high transition to the point of the output crossing TTL threshold in a low to high transition.

t_{pd-} (D) Latch Disable to Output Low Delay: The propagation delay measured from the latch signal crossing the TTL threshold in a low to high transition to the point of the output crossing TTL threshold in a high to low transition.

t_s **Minimum Setup Time:** The minimum time before the negative transition of the latch signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time:** The minimum time after the negative transition of the latch signal that an input signal must remain unchanged in order to be acquired and held at the output.

t_{pw} (D) **Minimum Latch Disable Pluse Width:** The minimum time that the latch signal must remain high in order to acquire and hold an input signal change.

High-Speed, Low-Power Voltage Comparators

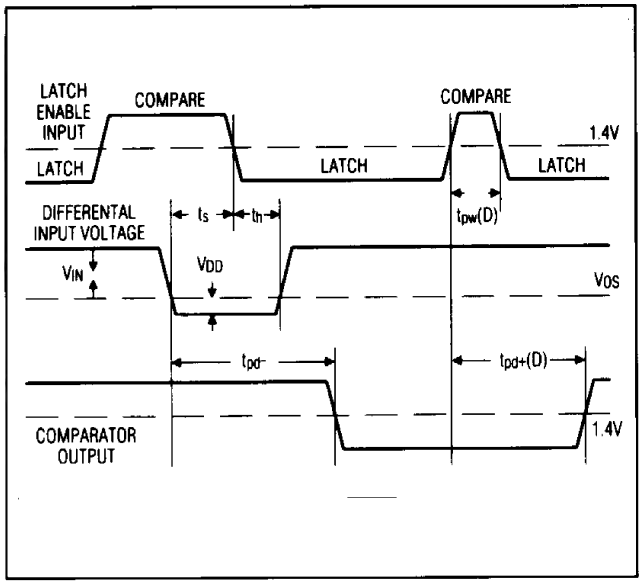


Figure 2. MAX900/902/903 Timing Diagram

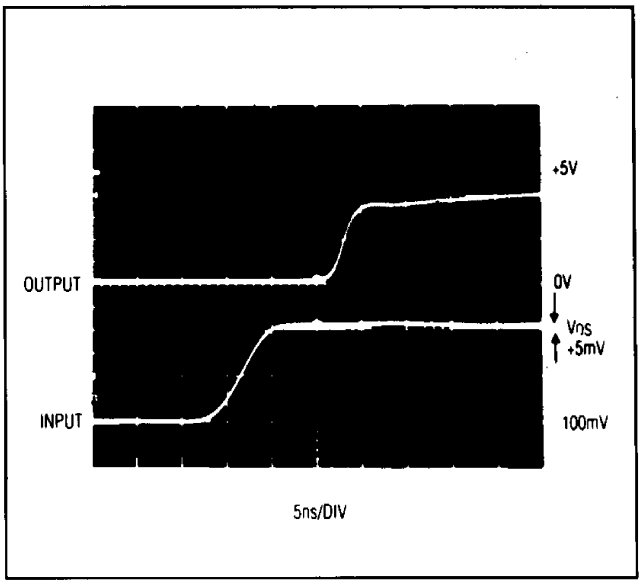


Figure 3. t_{pd}+ Response Time to 5mV Overdrive

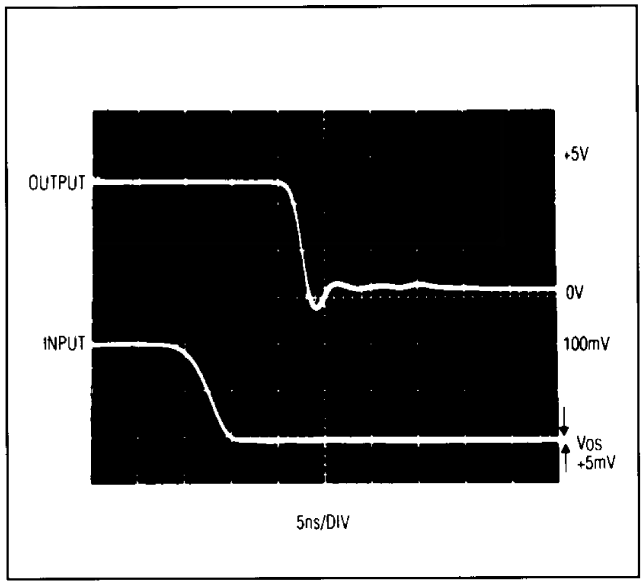


Figure 4. t_{pd}- Response Time to 5mV Overdrive

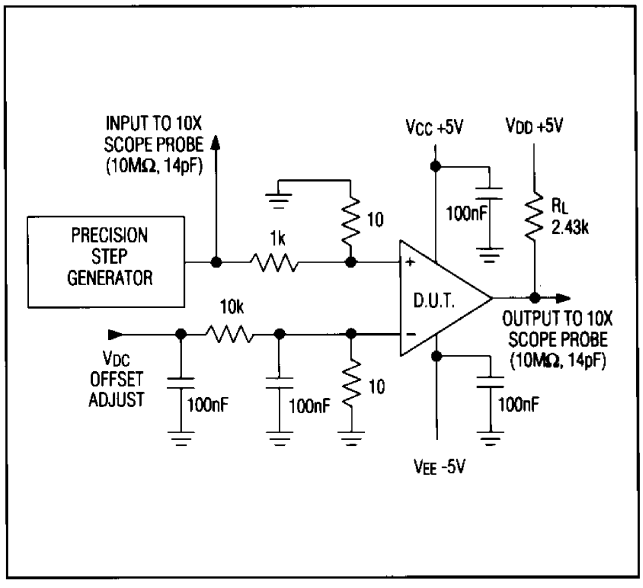


Figure 5. Response-Time Setup

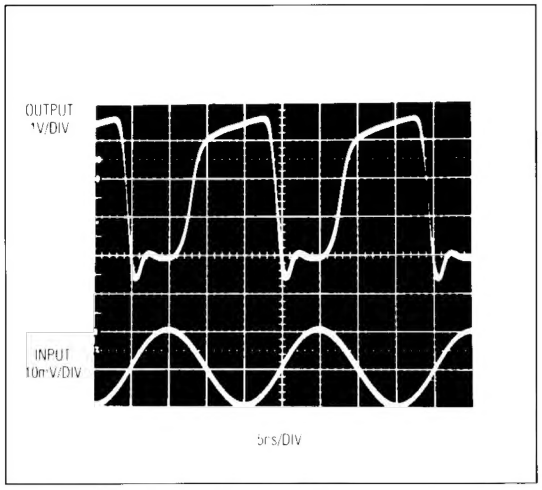


Figure 6. Response to 50MHz Sine Wave

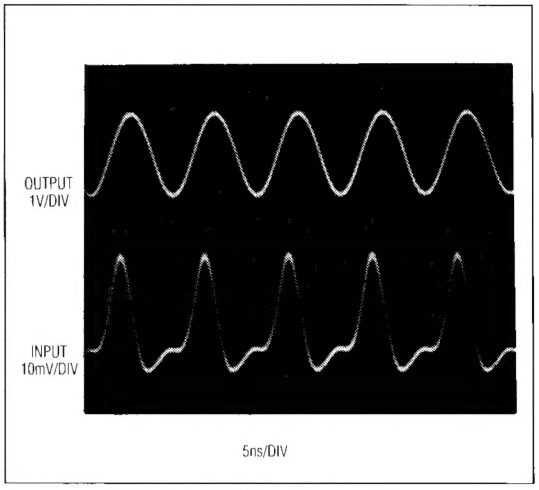


Figure 7. Response to 100MHz sine wave photo

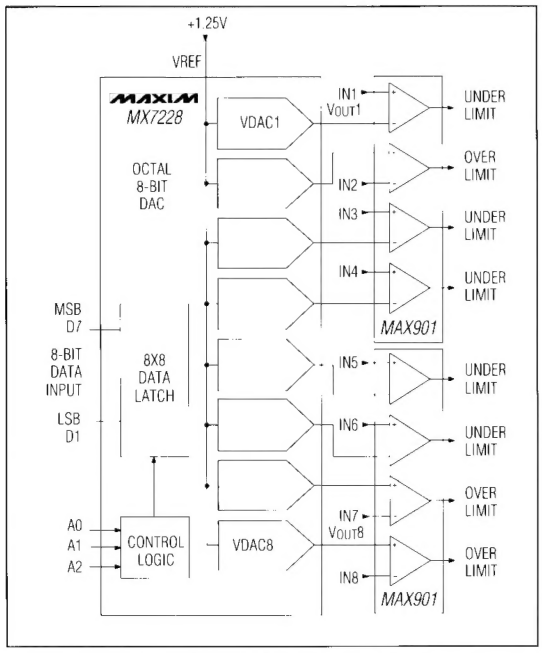


Figure 8. Alarm Circuit Level-Monitors Eight Separate Inputs

Typical Application

Programmed, Variable-Alarm Limits

By combining two quad analog comparators with an octal, 8-bit D/A converter (the MX7228), several alarm and limit-defect functions can be performed simultaneously without external adjustments.

The MX7228's internal latches allow the system processor to set the limit points for each comparator independently and update them at any time. Set the upper and lower thresholds for a single transducer by pairing the D/A converter and comparator sections.

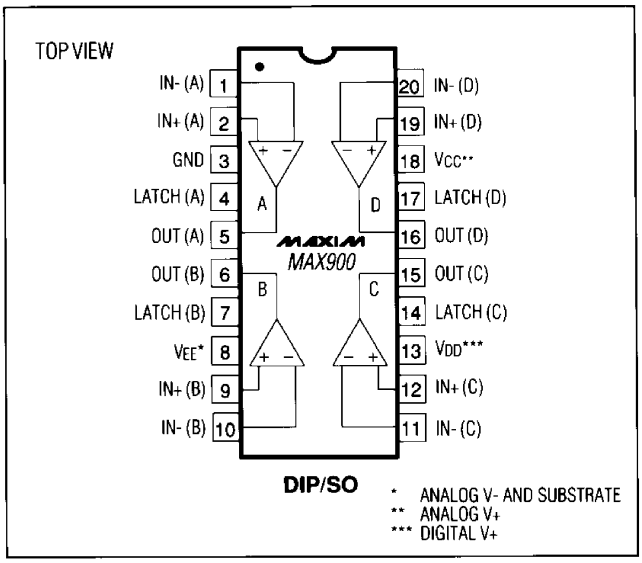
High-Speed, Low-Power Voltage Comparators

Ordering Information (continued)

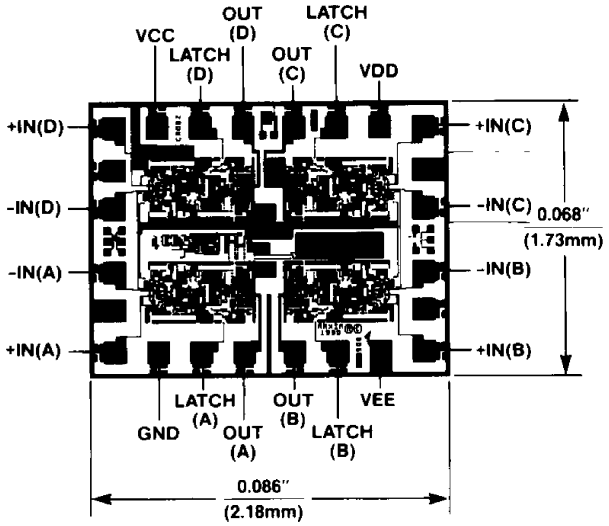
PART	TEMP. RANGE	PIN-PACKAGE
MAX901ACPE	0°C to +70°C	16 Plastic DIP
MAX901BCPE	0°C to +70°C	16 Plastic DIP
MAX901ACSE	0°C to +70°C	16 Narrow SO
MAX901BCSE	0°C to +70°C	16 Narrow SO
MAX901BC/D	0°C to +70°C	Dice*
MAX901AEPE	-40°C to +85°C	16 Plastic DIP
MAX901BEPE	-40°C to +85°C	16 Plastic DIP
MAX901AESE	-40°C to +85°C	16 Narrow SO
MAX901BESE	-40°C to +85°C	16 Narrow SO
MAX901AMJE	-55°C to +125°C	16 CERDIP
MAX901BMJE	-55°C to +125°C	16 CERDIP
MAX902CPD	0°C to +70°C	14 Plastic DIP
MAX902CSD	0°C to +70°C	14 Narrow SO
MAX902C/D	0°C to +70°C	Dice*
MAX902EPD	-40°C to +85°C	14 Plastic DIP
MAX902ESD	-40°C to +85°C	14 Narrow SO
MAX902MJD	-55°C to +125°C	14 CERDIP
MAX903CPA	0°C to +70°C	8 Plastic DIP
MAX903CSA	0°C to +70°C	8 SO
MAX903C/D	0°C to +70°C	Dice*
MAX903EPA	-40°C to +85°C	8 Plastic DIP
MAX903ESA	-40°C to +85°C	8 SO
MAX903MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

Pin Configurations (continued)



Chip Topography



Note: Substrate connected to V_{EE}.
MAX900/901/902/903